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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,498	07/29/2003	Shohci Osawa	2936-0191P	5056
2292	7590	05/25/2007		
BIRCH STEWART KOLASCH & BIRCH			EXAMINER	
PO BOX 747			MUI, GARY	
FALLS CHURCH, VA 22040-0747				
			ART UNIT	PAPER NUMBER
			2616	
			NOTIFICATION DATE	DELIVERY MODE
			05/25/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary

Application No.

10/628,498

Applicant(s)

OSAWA ET AL.

Examiner

Gary Mui

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5, 25, 30 and 32 is/are allowed.
- 6) ☒ Claim(s) 1, 6, 11, 14, 29 and 31 is/are rejected.
- 7) ☒ Claim(s) 2-4, 7-10, 12, 13, 15-24 and 26-28 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 29 July 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. Figures 32 – 41 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. In addition to Replacement Sheets containing the corrected drawing figure(s), applicant is required to submit a marked-up copy of each Replacement Sheet including annotations indicating the changes made to the previous version. The marked-up copy must be clearly labeled as “Annotated Sheets” and must be presented in the amendment or remarks section that explains the change(s) to the drawings. See 37 CFR 1.121(d)(1). Failure to timely submit the proposed drawing and marked-up copy will result in the abandonment of the application.

Specification

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Kalkunte et al. (US 6,108,306).

For claim 1, Kalkunte et al. teaches a plurality of ports of different types; a bus arbitration circuit that controls timing with which signals are output from the individual ports to a serial bus; a register in which are stored conditions under which the bus arbitration circuit should operate; and a delay value optimizing processor that monitors the individual ports and optimizes a transmission delay value of the transmitter/receiver apparatus according to operation status of the individual ports (see column 4 lines 28 – 44 and column 6 line 59 – column 7 line 24, the controller controls the bandwidth of each port based on condition of the network capacity and port activity, the MAC will receive this bandwidth information and stores it in a register to control the data rate of the data packet, the timer will calculate the delay value).

For claim 29, Kalkunte et al. teaches a communication line by way of which communication is conducted with an external node complies with one of IEEE Std. 1394a-2000, IEEE Std. 1394b, or the OP i.LINK standard (see column 3 line 62 – column 4 line 3).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over by Kalkunte et al.

For claim 6, Kalkunte et al. a plurality of ports of different types; a bus arbitration circuit that controls timing with which signals are output from the individual ports to a serial bus; a first register in which a first operation condition of the bus arbitration circuit is stored; a delay value optimizing processor that monitors the individual ports and optimizes a transmission delay value of the transmitter/receiver apparatus according to operation status and type of the individual ports. Kalkunte et al. fails to teach a second register in which a second operation condition of the bus arbitration circuit is stored. It is obvious to one of ordinary skill in the art at the time of the invention was made to duplicate the first register to have a second register to hold operation condition. The motivation for doing this is to have a more versatile system.

Claim Rejections - 35 USC § 103

11. Claims 11, 14 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Kalkunte et al. in view of Scott (US 2005/0007952 A1).

For claim 11, Kalkunte et al. teaches a plurality of ports of different types; a bus arbitration circuit that controls timing with which signals are output from the individual ports to a serial bus; a register in which are stored conditions under which the bus arbitration circuit should operate (see column 4 lines 28 – 44 and column 6 line 59 – column 7 line 24, the controller controls the bandwidth of each port based on condition of the network capacity and port activity, the MAC will receive this bandwidth information and stores it in a register to control the data rate of the data packet). Kalkunte fails to teach a jitter value optimizing processor that monitors the individual ports and optimizes a jitter value of the transmitter/receiver

apparatus according to operation status of the individual ports. Scott from the same field of endeavor teaches the traffic analyzer includes an input port, a calculator, a sliding window, and an output port. For example, input port is coupled to calculator. Calculator is coupled to sliding window array and output port. For clarity, the operation of the traffic analyzer is further described with respect to routine for analyzing traffic (FIG. 8). Input port receives traffic (from the framer. In one embodiment, the traffic is a stream of in-order, time-stamped, indexed packets. Calculator calculates the jitter and jitter variation for each received packet (step 810). For example, one way of calculating jitter is to take the absolute value of the difference between the actual interpacket time and the theoretical interpacket time. The interpacket time is width in terms of time of a packet. For instance, a 30 ms packet has a theoretical interpacket time of 30 ms. This same packet may not arrive at the destination gateway with the same interpacket time. Thus, jitter is the difference between the actual or received interpacket time and its theoretical value (see paragraph 0057). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to monitor the ports for jitter value as taught by Scott into network switch of Kalkunte et al. The motivation for doing his is to have a more efficient system.

For claim 14, Kalkunte et al. teaches a plurality of ports of different types; a bus arbitration circuit that controls timing with which signals are output from the individual ports to a serial bus; a first register in which a first operation condition of the bus arbitration circuit is stored; stored. Kalkunte fails to teach a second register in which a second operation condition of the bus arbitration circuit is a jitter value optimizing processor that monitors the individual ports and optimizes a jitter value of the transmitter/receiver apparatus according to operation status

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and type of the individual ports. Scott from the same field of endeavor teaches the traffic analyzer includes an input port, a calculator, a sliding window, and an output port. For example, input port is coupled to calculator. Calculator is coupled to sliding window array and output port. For clarity, the operation of the traffic analyzer is further described with respect to routine for analyzing traffic (FIG. 8). Input port receives traffic (from the framer. In one embodiment, the traffic is a stream of in-order, time-stamped, indexed packets. Calculator calculates the jitter and jitter variation for each received packet (step 810). For example, one way of calculating jitter is to take the absolute value of the difference between the actual interpacket time and the theoretical interpacket time. The interpacket time is width in terms of time of a packet. For instance, a 30 ms packet has a theoretical interpacket time of 30 ms. This same packet may not arrive at the destination gateway with the same interpacket time. Thus, jitter is the difference between the actual or received interpacket time and its theoretical value (see paragraph 0057). It would also be obvious to one of ordinary skill in the art at the time of the invention was made to duplicate the first register to have a second register to hold operation condition. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to monitor the ports for jitter value as taught by Scott into network switch of Kalkunte et al. The motivation for doing his is to have a more efficient and versatile system.

For claim 31, Kalkunte et al. teaches a communication line by way of which communication is conducted with an external node complies with one of IEEE Std. 1394a-2000, IEEE Std. 1394b, or the OP i.LINK standard (see column 3 line 62 – column 4 line 3).

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Allowable Subject Matter

12. Claims 5, 25, 30, and 32 are allowed.
13. Claims 2 – 4, 7 – 10, 12, 13, 15 – 24, and 26 – 28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

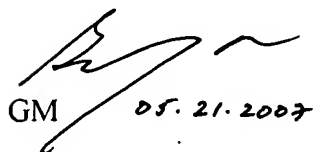
14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Bonomi et al. (US 5,838,681), Goel et al. (US 6,661,797 B1), Gibson et al. (US 6,680,908 B1), Ueno (US 6,751,197 B1), and Bordonaro et al. (US 2006/0239204 A1) are cited to show a Transmitter/receiver apparatus.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary Mui whose telephone number is (571) 270-1420. The examiner can normally be reached on Mon. - Thurs. 9 - 3 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on (571) 272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


GM 05.21.2007


RICKY Q. NGO
SUPERVISORY PATENT EXAMINER